The UC3848 Average Current Mode Controller Squeezes Maximum Performance from Single Switch Converters

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ABSTRACT

This application note describes the UC3848 average current mode PWM controller. The unique features of this controller are discussed, which make primary side average current mode control practical for isolated converters. The UC3848 employs a current waveform synthesizer which monitors switch current and simulates the inductor current down slope, generating a complete current waveform without actual secondary side measurement. Primarily intended for single ended converters, several additional features such as accurate duty-cycle and volt-second limiting allow maximum transformer and switch utilization. A three output, 200 watt off-line design example is presented which also features planar magnetics and a coupled output inductor.

INTRODUCTION

The UC3848 represents a significant advance in the control of single switch forward converters. Generally considered simple and reliable, but non-optimum in transformer and switch utilization, the single switch forward has previously been reserved for less demanding applications. Upon careful examination however, it is apparent that many of the perceived limitations actually result from the control circuitry rather than the converter topology itself.

The advantages that an inner current loop brings to power supply design and performance are well known [1]. Current mode control is usually preferred over direct duty cycle control because of the superior input supply rejection and simplified voltage loop closure. Average current feedback provides additional advantages over the more common peak current feedback. Major benefits include inherent slope compensation, better noise rejection, and the ability to operate with both continuous and discontinuous inductor current. Additionally, average current feedback provides significantly better closed current loop accuracy. This further improves input supply rejection and current limit accuracy. Average current feedback is detailed in the references [2,3,4].

Maximum power component utilization requires carefully defined and controlled operating mode boundaries. While this can be said of many converter topologies, it is particularly critical with the single switch forward because of the transformer reset mechanism. Energy in the transformer leakage and magnetizing inductance must be removed after each energy transfer cycle. Above all, the control circuit must insure that this condition is achieved. Total losses are generally minimized by bringing the peak power transfer as close to the average as possible. This indicates that improvements in efficiency and component utilization are obtainable by maximizing duty-cycle. Unfortunately, maximizing duty-cycle conflicts with assuring transformer reset, traditionally requiring an overly conservative design to assure reliability.

Previously, these characteristics have limited the single switch converter to low-power, low-end applications. The UC3848 Average Current Mode PWM Controller allows operation beyond conventional limitations by employing highly accurate circuitry to provide programmable operating boundaries, and by implementing an inner average current feedback loop for improved control characteristics and accuracy. This control circuit advance capitalizes on unique, patented circuitry, and the precision achievable with Unitrode's thin-film resistor process.

The UC3848 Average Current Mode PWM Controller

The block diagram of the UC3848 shown in figure 1, illustrates a number of unique functions. Although the IC can certainly be used for flyback,

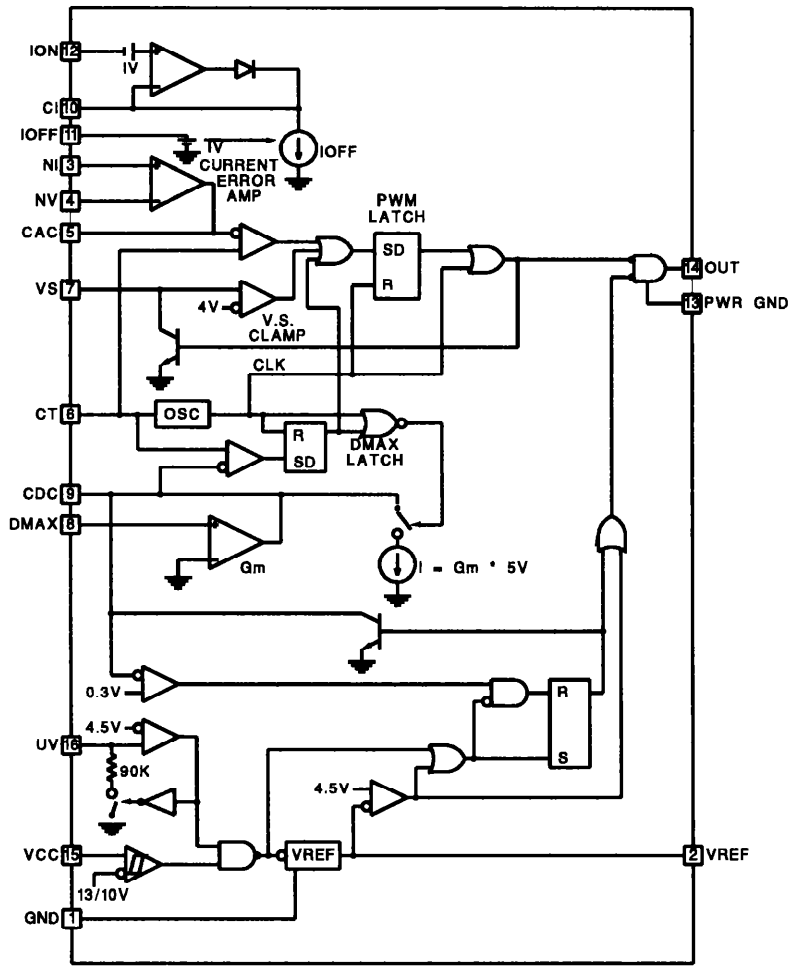

Figure 1

UC3848 Average Current Mode PWM Controller

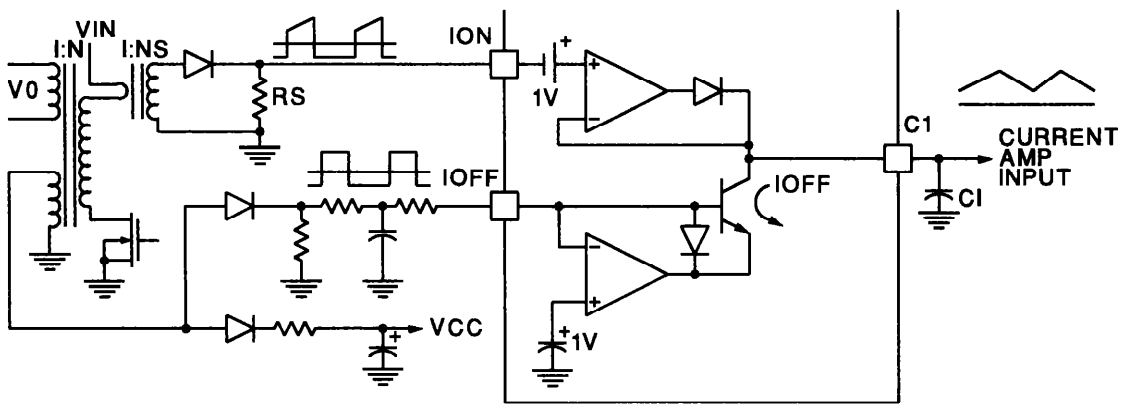

Figure 2

Inductor Current Waveform Synthesizer

boost, as well as other buck derived converters [4], the UC3848 has been optimized for forward converter use. The UC3848s precision functions bring switching power supply control to a new level:

- Average Current Mode Control
- Average Current Sense Signal Synthesizer
- Programmable Maximum Duty-Cycle and Volt-Second Control
- Under Voltage Lockout (UVLO) monitors Vcc, Vin, and Vref
- 2 Amp peak MOSFET Driver with Active Low During UVLO
- 8MHz gain-bandwidth Current Error Amplifier
- Latched PWM comparator
- Practical Operation up to 1 MHz
- Low Start-Up Current (500uA)
- Precision Reference (1% @ 5V)

The sophistication and performance of the UC3848 may at first appear contradictory to simple forward converter design. A truly simple implementation however, is best achieved by maintaining simple power circuitry, and p/acing the complexity and precision in the control circuitry where it can be integrated into a single IC.

Average Current Mode Control

Average current loop implementation first requires an average current signal for the control variable. This immediately presents a problem with isolated converters since this signal is entirely on the secondary side. A current sense transformer cannot be used to directly sense output inductor current with buck derived converters since the inductor normally has a continuous DC component. A potentially complex and expensive solution is avoided with the realization that output inductor current is directly reflected to the primary during the switch on time. Simply scaling the switch current by the transformer turns ratio provides the rising portion of the inductor current waveform. When the switch is off, the inductor current decays at V_{OUT}/L. This information can be used to synthesize an analog of the actual output inductor current without any secondary connections.

Inductor current is synthesized by the UC3848 with a circuit that behaves similar to a track and hold amplifier, as shown in figure 2. While the switch is on, a unity gain buffer charges an external capacitor (C_I), essentially following the rising input current waveform. A one volt offset is also added to provide sufficient headroom for the buffer's output stage. When the switch turns off, a programmable current sink discharges the capacitor, simulating the actual inductor current decay. Several techniques are available for setting the discharge current, depending on the required accuracy of the current sense signal. If good short-circuit accuracy is required, an analog of the output voltage is required to control the synthesizer capacitor discharge rate. There are two simple ways to derive this signal on the primary side.

The first method uses a transformer bootstrap winding voltage as shown in figure 2. The average value of the rectified output and bootstrap winding voltages are directly proportional. By adding a separate rectifier and filter to this winding, the capacitor discharge current can be programmed to track V_{OUT}. Typically, a bootstrap winding is employed with off-line converters to power the control circuitry after initial start-up, so the raw signal is usually present at no additional cost. Note that an error is present during transients since the filter creates a lag between the output and the filtered bootstrap voltages.

If the transient error is unacceptable, the technique shown in figure 3 can be used. A secondary winding on the output inductor provides a voltage directly proportional to the output without filtering. While the switch is off, V_{OUT} is across the output inductor. Any other winding on the inductor will have a voltage proportional to V_{OUT} by the turns

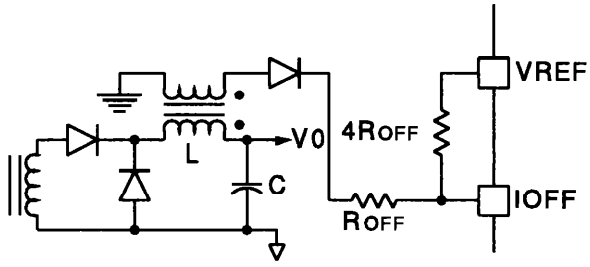

Figure 3
IOFF Generation using
Second Inductor Winding

ratio of the two windings. The sense winding rectifier drop cancels the output rectifier drop when the turns ratio is 1 : 1, yielding excellent signal accuracy. While this approach is simple and accurate, it does come at additional expense since this winding is not normally required. Additionally, high voltage agency approved isolation is required for off-line converters, adding further cost and manufacturing complexity to the inductor.

With either of these techniques, an offset current may be added to compensate for the synthesizer's

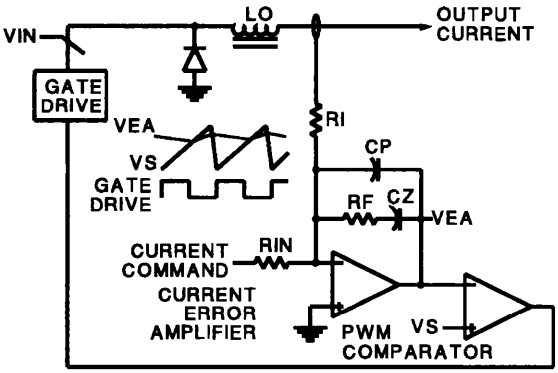

FIGURE 4. AVERAGE CURRENT FEEDBACK LOOP

Figure 4

Average Current Feedback Loop

one volt offset. Connecting a resistor with a value four times the I_{OFF} input resistor between the V_{REF} and I_{OFF} pins cancels the offset.

Often, a fixed discharge current is acceptable. This is programmed by connecting a resistor between the V_{REF} and I_{OFF} pins. The synthesized current waveform is quite accurate when the output voltage is near the regulating value, however an error exists during start-up and output short-circuit. During a short, the current decays much slower since V_{OUT} is only the output rectifier and circuit resistance voltage drops. The current ripple also becomes a small fraction of its value at the regulating voltage. The synthesizer however, discharges the capacitor as if the output were not shorted, and therefore underestimates the output inductor current. The short-circuit current will then exceed the programmed limit by almost one-half of the normal peak-to-peak ripple current. Typically, the inductor ripple current is 20% to 30% of the maximum DC value, corresponding to a short circuit current 10% to 15% higher than the maximum output current available at normal output voltage.

The current error amplifier has sufficient gain to use a current sense resistor directly in most applications. A current sense transformer however, results in better performance by allowing a larger amplitude, lower noise signal. Ideally, the current sense signal is scaled to 4 volts at the maximum current level. The current transformer load resistance is then:

$$R_S = 4V \times N \times \frac{N_S}{I_L} \qquad (1)$$

where N = transformer turns ratio
N_s = current transformer ratio
I_L = maximum load current

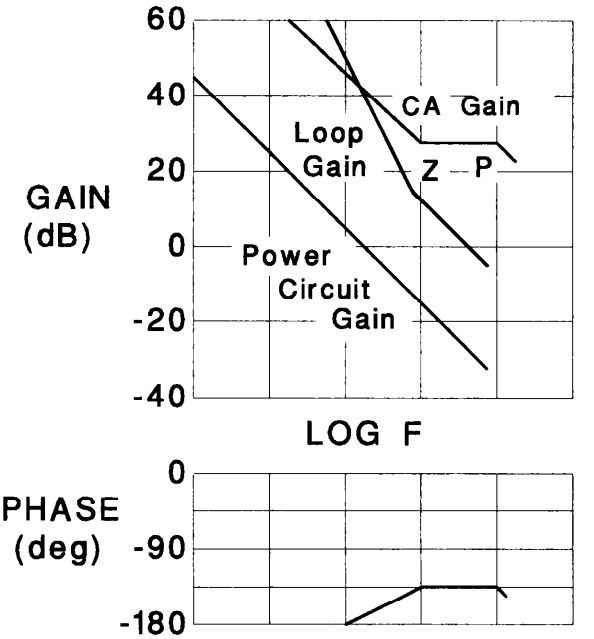

Figure 5

Open Current Loop Response

With multiple secondaries, normalize all other loads to the main output through the turns ratio directly. Note that for these calculations, output inductors and their effect on ripple current is not considered, since the UC3848 controls average, not peak current. Output inductances must be normalized to the main output through the turns ratio squared however, when calculating peak current and current ripple.

The recommended nominal I_{OFF} current is 100µ A, leaving C_I the remaining current synthesizer component.

$$C_I = \frac{(100\mu A \times N \times N_S \times L_{NORM})}{(Rs \times V_{OUT}(nom))} \qquad (2)$$

where L_{NORM} = normalized output inductance

Figure 4 shows the average current feedback loop. This inner loop is analogous to direct duty-cycle or voltage-mode control except that the control variable is output inductor current rather than output voltage. Properly compensated, the open loop gain is comparable to peak current-mode's at high frequency, and becomes orders of magnitude higher as frequency decreases. The open current loop response shown in figure 5 illustrates this behavior. This high open loop gain translates into high

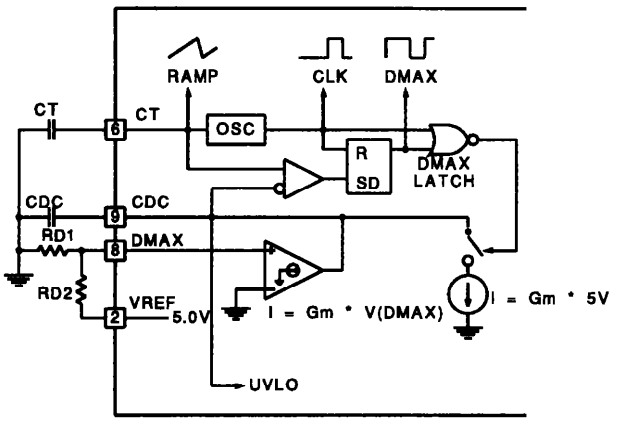

Figure 6

Duty-Cycle Limit Programming

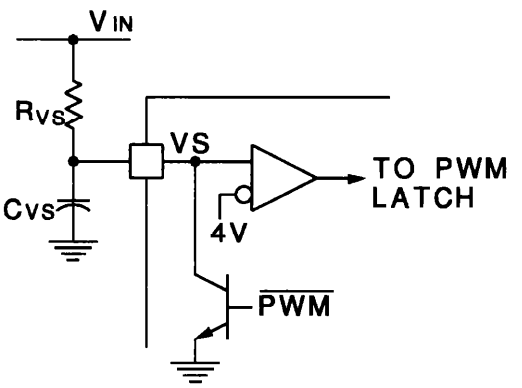

Figure 7

Volt-Second Clamp

closed loop accuracy. In comparison, peak current mode relies entirely on its transfer function accuracy, and has no means by which to reduce errors. This characteristic difference from peak current-mode is attributed to the current error amplifier's compensation, and is key to the resulting performance enhancements.

The increased gain at low frequency provides excellent closed current loop accuracy, even when the inductor current becomes discontinuous. High open loop gain also allows greater filtering of the current sense signal with no degradation in closed loop accuracy. It is this characteristic, along with the larger amplitude signals that provides significantly reduced noise susceptibility in comparison to peak current-mode control.

PWM Oscillator

Oscillator programming is simplified by providing internally set charge and discharge currents. Excellent initial accuracy and temperature stability are assured by precision thin-film resistors. Since only a timing capacitor (C_T) is required to set the frequency, external component error contribution is minimal. The precision high speed oscillator combined with short propagation delay through the PWM circuitry allows practical operation up to 1MHz.

A 200µA charge current and a 1800µA discharge current generates a sawtooth waveform with a well defined rise/fall relationship and accurate frequency. During discharge, the output driver is disabled, limiting the maximum duty-cycle to 90%. Note that this maximum can be reduced by the accurate, duty-cycle limit and the volt-second product limit circuits, which are explained in following sections. Oscillator frequency is programmed by:

$$F = \frac{1}{(10k \times C_T)} \quad (3)$$

If greater frequency accuracy is required, a trim resistor in parallel with C_T can be added to lower the frequency. The trim resistor should not be less than 40kΩ, limiting the maximum trim range to 25% below nominal. Frequency decrease as a function of trim resistance is shown on the UC3848 data sheet.

Duty-Cycle Limiting and Soft Start

The conventional single switch forward converter design usually limits the maximum duty-cycle to 50%. This limit however, is only required if a one-to-one clamp winding is employed to facilitate transformer core reset. While some designers still use this technique, a resistor/capacitor/diode (RCD) clamp has become more prevalent. The RCD clamp eliminates a transformer winding and potentially offers a wider duty-cycle range. Currently, a 50% duty-cycle limit is primarily used because it can be accurately derived from a toggle flip-flop. To exploit a wider duty-cycle, an accurate, programmable duty-cycle clamp is required.

The UC3848 employs a unique, patented technique to limit the maximum duty-cycle to a value programmed by a resistive divider. The circuit utilizes a capacitor (C_{DC}) for integration only, and does not rely on its absolute value for maximum duty-cycle accuracy. The absolute value of C_{DC} does set the soft-start time constant, although high precision is not normally required for this function.

Internally, the UC3848 capitalizes on the excellent matching characteristics achievable on an IC to implement a charge balanced loop. A matched transconductance source and sink form a precision integrator circuit, as shown in figure 6. The current

source is externally programmed to Gm x V_{DMAX} and is on continually. The current sink is internally set at Gm x 5V, and is switched on and off. The resulting discharge current is Gm(5V - $_{DMAX}$). The current source and sink charge and discharge C_{DC}, while its voltage is compared with the oscillator voltage.

The current sink discharges C_{DC} from the time that the switch is turned on until the oscillator voltage becomes greater than C_{DC}'s voltage. For the remainder of the period, C_{DC} is charged by the current source. Note that C_{DC}'s voltage is essentially a DC level with a very small ripple component unless it is a particularly small value. C_{DC} maintains a constant voltage only if the average applied charge is zero. The charge balanced loop therefore forces $I_{DISCHARGE} \times T_{ON(max)}$ to equal $I_{CHARGE} \times T_{OFF(min)}$. A large offset voltage between C_T and C_{DC} may be observed when measuring an actual circuit. This offset contributes negligible error since high DC loop gain reduces its effect by several orders of magnitude.

While the circuit's operation may seem complicated, it couldn't be easier to apply. A voltage divider from V_{REF} to D_{MAX} as shown if figure 6 sets the maximum duty-cycle. The circuit inherently provides soft-start at initial power-up as C_{DC} charges to it's steady state value. Increasing C_{DC} extends the loop settling time, and hence the soft-start time constant, with no effect on the programmed maximum duty-cycle. Note that the single pole loop response avoids overshoot, regardless of the integrating capacitor value. Soft-start after fault is explained in the under-voltage lockout section. Maximum duty-cycle and soft-start are programmed by the following relationships:

$$D_{MAX} = \frac{R_{D1}}{(R_{D1} + R_{D2})} \quad (4)$$

$$\tau_{ss} = 20k \times C_{DC} \quad (5)$$

Volt-Second Product Limit

During transients it may be desirable to limit the duty-cycle below the programmed maximum value. For example, active transformer reset circuits vary the clamp voltage inversely proportional to the input supply voltage [5]. During steady state operation the peak MOSFET voltage varies much less than with passive clamp circuits. Unless the input voltage range is large, the peak MOSFET voltage will be fairly constant. This occurs because the applied volt-second product remains constant over the entire operating duty-cycle range during steady state. Thus as the input voltage goes up and the duty-cycle decreases, the clamp voltage goes down as the reset time increases.

If during a transient the duty-cycle is allowed to increase excessively, the MOSFET will be subjected to significantly higher voltages. This assumes that the reset circuit's clamp voltage can slew rapidly. If it cannot, the magnetizing current will ratchet up, possibly saturating the transformer. Both scenarios are easily prevented by simply limiting the maximum applied volt-second product.

The UC3848 generates a voltage proportional to the volt-second product with the circuit shown in figure 7. A current directly proportional to the supply voltage (V_{IN}/R_{VS}) charges a capacitor (C_{VS}) while the MOSFET is on. When the MOSFET is turned off, the capacitor is discharged. Volt-second limiting is accomplished by comparing the capacitor's voltage to a 4 volt reference, and terminating the pulse width for the remainder of the switching period. Normally, the worst case MOSFET voltage occurs during maximum input voltage at the volt-second limited duty-cycle. However, high turns ratio designs which allow a very wide duty-cycle may actually generate the highest MOSFET voltage during low-line at the volt-second limited duty-cycle.

Since the volt-second product is constant it can be calculated at any input voltage. The effectiveness

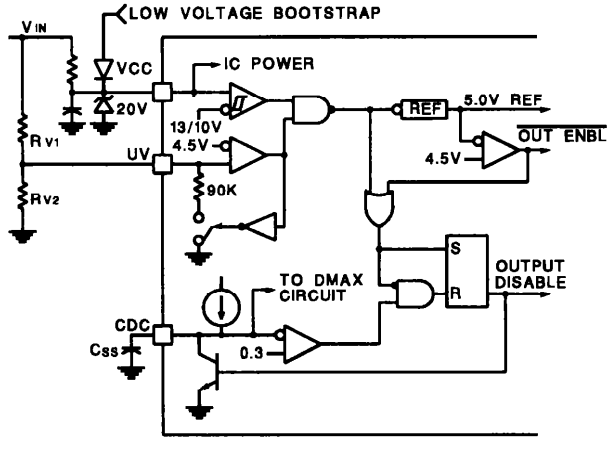

Figure 8

Under Voltage Lockout

of the volt-second limit however, should be analyzed at minimum and maximum input voltage, in addition to a few more typical voltages. The volt-second product clamp is programmed by:

$$V_{IN} \times T_{ON} = 4.0V \times R_{VS} \times C_{VS} \quad (6)$$

Under Voltage Lockout

Programmable under voltage lockout (UVLO) further defines operating mode boundaries. V_{CC}, V_{IN},

and V_{REF} are monitored to insure that the chip supply, main input supply, and reference are within specification before enabling the output stage. Figure 8 shows the block diagram of the UVLO circuitry.

The V_{CC} comparator monitors the chip supply voltage. Hysteretic thresholds at 13V and 10V insure that sufficient voltage is available to power the chip and fully turn on the MOSFET. The V_{IN} comparator monitors the input supply through a resistive divider. A small capacitor from UV to ground is usually required to filter noise from this high impedance node. Both the thresholds and the hysteresis are programmed by the divider values with the relationships:

$$V_{IN(ON)} = 4.5V \times \left(1 + \frac{R_{V1}}{R_{V2'}}\right) \quad (7)$$

$$V_{IN(OFF)} = 4.5V \times \left(1 + \frac{R_{V1}}{R_{V2}}\right) \quad (8)$$

where $R_{V2'} = R_{V2} \parallel 90k$

$$V_{IN(HYS)} = 4.5V \times \frac{R_{V1}}{90k} \quad (9)$$

When either the V_{CC} or the V_{IN} comparator are low, the bias circuitry to the rest of the chip is off. The quiescent current (loo) is nominally 500µ A to facilitate off-line applications. Once both V_{CC} and V_{IN} are within specification, the bias circuitry for the rest of the chip is activated. The output driver and C_{DC} pin are still held low until V_{REF} exceeds the 4.5V threshold of the V_{REF} comparator. When the V_{REF} comparator goes high, control of the output driver transfers to the PWM circuitry and C_{DC} is allowed to charge, soft-starting the supply.

If any of the three monitored voltages falls below their threshold during start-up or normal operation, the UVLO latch is set, the output driver is held low, and C_{DC} is discharged. This state is maintained until C_{DC} is fully discharged, at which point operation is as described above.

Output Driver

High current transistors enable the output driver to deliver 2 amps peak allowing direct interface to any MOSFET typically used in single ended converters. The driver also incorporates self-biasing circuitry that maintains a low impedance to ground during UVLO. This assures that high dv/dt at V_{IN} during power-up cannot inadvertently turn on the MOSFET through its miller capacitance.

The combination of high peak current, stray circuit inductance, and capacitive gate load result in reflections back to the driver, which if left unclamped, will cause erratic chip behavior. External schottky diodes from the output to V_{CC} and ground will divert the reflected current and assure reliable operation. A well designed layout with typical circuit values will normally require 1A, 20V schottky clamp diodes. Looser layouts, longer gate drive traces, and lower gate resistor values all place greater demand on the output clamping circuit, and may necessitate higher current diodes.

Voltage Reference and Error Amplifier

Since the UC3848 is intended for primary side control, the voltage reference (V_{REF}) does not affect output voltage stability. It does however, affect current limiting and the other precision circuits previously mentioned, and has therefore been designed for good initial accuracy and temperature drift. The reference should be capacitively bypassed to reduce high frequency output impedance and noise susceptibility.

To facilitate wide bandwidth current loops, the error amplifier has an 8Mhz gain bandwidth product. Even with small current feedback signals such as from a current sense resistor, loop bandwidth will almost always be limited by external circuit characteristics rather than error amplifier limitations. The amplifier's 8 V/s slew rate assures that even during large signal transients, external components will determine circuit behavior.

Design Example

A 200 watt off-line supply utilizing the UC3848 is shown in figure 9. It delivers a regulated +5V at 20A, and a semi-regulated +/-15V at 3.3A. The conversion frequency is 260kHz, which was determined to be a reasonable compromise between size and efficiency. A coupled output inductor improves dynamic cross regulation and steers some of the +5V ripple current to the +/-15V filter capacitors [9]. This results in minimal total output capacitor volume. A bridge/doubler input rectifier allows operation over an input range of 85 to 265VAC. For simplicity and cost, an RCD clamp is employed to facilitate transformer reset. This common configuration is typical of many commercial applications.

The transformer turns ratio is selected to minimize MOSFET stress. Ideally, the maximum duty-cycle should be as large as possible, allowing the highest turns ratio and lowest reflected load current. This must be balanced against the peak MOSFET voltage developed during transformer reset.

Since the UC3848 can accurately define operating mode boundaries, any practical duty-cycle range can be used. This allows maximum utilization of both current and voltage capability of a particular

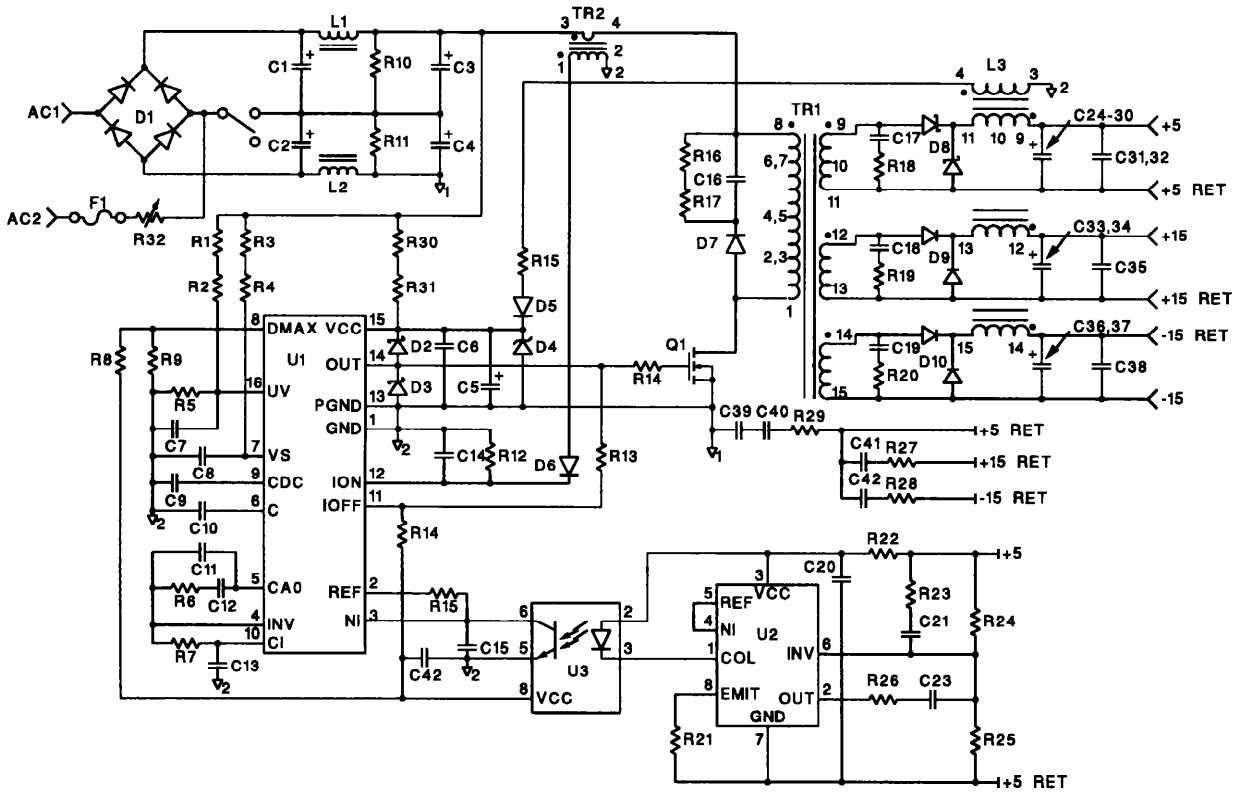

Figure 9

200W 3 OUTPUT FORWARD CONVERTER

MOSFET. The RCD clamp allows some trade-off in dissipation versus peak MOSFET voltage. Turns ratio and clamp optimization requires a good estimation of leakage inductance, switch capacitance, and transformer interwinding capacitance, since energy stored in these parasitics will be transferred or dissipated each switching cycle. RCD clamp optimization is covered in detail in reference [6].

The design example transformer uses a 16:1 turns ratio (primary to 5 volt), allowing a wide input supply range and reliable use of an 800V MOSFET. The MOSFET, an APT801R2BN from Advanced Power Technology [7], is rated at 800V and has 1.2Ω maximum on resistance at 25°C. A planar transformer and coupled output inductor from Signal Transformer Co. [8] are used, which offer several advantages over custom wound components. Planar construction provides tighter parameter tolerance. Compact, low profile magnetics help achieve high power density. Their standard design provides agency approved insulation and known performance characteristics, greatly reducing the number of iterations to produce a good power supply design.

The duty-cycle is limited to 0.6, maintaining regulation down to approximately 160 VDC in. With the switching frequency programmed for 260 kHz, the nominal volt-second product is 345 Vs. The volt-second clamp is programmed to 425 Vs to allow for tolerances and large signal transients.

A current transformer senses switch current resulting in minimal loss and good signal quality. A 1000pF capacitor shunts the high frequency turn-on spike before feeding the current sense signal to the UC3848s current waveform synthesizer. A fixed I_{OFF} value renders an acceptable short circuit current for this application. Average short circuit losses are kept low by the hiccup action which occurs as the boot-strap supply collapses and the supply restarts. Highly accurate short circuit current is most advantageous when a continuous supply is available for the control circuit such as in low voltage DC to DC converter applications.

When the MOSFET is on, the current synthesizer's I_{OFF} current is increased through a resistor connected to the gate driver output (R13). This allows C_I's voltage to better follow rectifier reverse recovery spikes present in the current waveform. This technique allows minimal filtering of the current

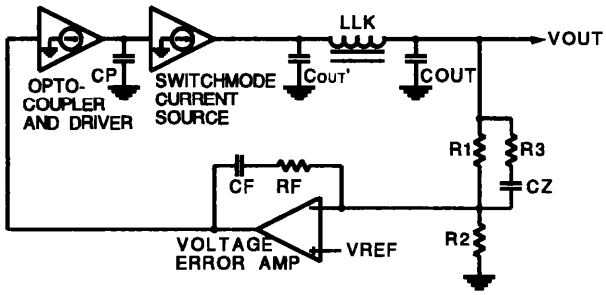

Figure 10

Voltage Feedback Loop

sense signal, and thus preserves accuracy.

The coupled output inductor provides good dynamic cross regulation, and steers some of the 5 volt ripple current to the +/-15 volt outputs where it is more efficiently filtered. Although this technique minimizes size and complexity, it does negate two major advantages of average current mode control. The average current loop maintains excellent regulation down to zero load for the fully regulated output. Unfortunately, the semi-regulated outputs will degrade quickly as the inductor current becomes discontinuous, forcing minimum loads for reasonable output voltage tolerance. Also, stray and leakage inductance between the secondary circuits introduces parasitic tank circuits, which if underdamped, will cause output ringing and instability. Generally, electrolytic output capacitors, low coupled inductor leakage inductance, and tight layout will allow successful implementation, although loop bandwidth must usually be compromised to maintain stability. Coupled output inductor design and application is detailed in reference [9].

Without the additional output circuitry parasitics, a single output supply with average current feedback has excellent regulation and transient response from zero to full load. There is also much less restriction on output capacitor type, allowing small ceramic or film capacitors in many applications. Although the design example's closed loop bandwidth is not as high as would be achievable with a single output, the electrolytic output capacitors store enough energy to provide good transient response and low output impedance.

Control Loops

A block diagram of the voltage feedback loop is shown in figure 10. For clarity, the inner average current feedback loop is shown as a transconductance amplifier, and is identical to figure 4. Current loop compensation is best described in the references [2,3], as a number of subtleties must be considered for optimal performance. The basic approach is easily summarized:

To avoid subharmonic oscillation of a single pole system, the amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input. This puts an upper limit on the current amplifier gain, and indirectly sets the loop gain crossover frequency. As derived in [2], the resulting unity gain crossover frequency will be:

$$f_C = \frac{(f_s V_{IN})}{(2\pi V_{OUT})} = \frac{f_s}{(2\pi D)} \quad (10)$$

The crossover frequency must be reduced in a practical system to account for tolerances and additional waveform slope injected by output voltage ripple through the voltage error amplifier. For the design example, f_C is approximately 50kHz at the maximum duty-cycle.

At the switching frequency, the average current loop's behavior is similar to peak current mode control. Placing a zero at one-half the crossover frequency increases the loop gain with decreasing frequency, providing high closed current loop accuracy. To further reduce noise susceptibility, a pole is placed at the switching frequency. While such a low frequency filter is completely unacceptable with peak sensing, the high gain at low frequency assures accurate current limiting. It is these fundamental differences from peak current mode which provide the performance enhancements.

The voltage loop reference and error amplifier reside on the secondary side as typically configured in off-line power supplies. A UC19432 incorporates a high precision reference, voltage error amplifier, and programmable transconductance amplifier for accurate opto-coupled feedback. Voltage loop compensation is normally the same as with peak current mode control and is described in detail in the references [2,9,10]. As previously noted, an additional LC pole resulting from leakage and stray inductance requires additional compensation. Ultimately, this parasitic restricts the bandwidth of this coupled inductor design example, although transient response is still quite good. The same control configuration with a single output supply provides optimal performance and allows simpler compensation.

Summary

The UC3848 clearly demonstrates the next level of switching power supply control achievable with improved techniques and precision circuitry. High

performance and high power density objectives coupled with the need for simplicity and low cost have called for further refinement of single switch conversion. The UC3848 answers that call combining precision circuitry, average current mode control and function flexibility, allowing optimal power component utilization and performance.

References:

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Unitrode Data Sheets:

UC3848
UC1 9432

PARTS LIST FOR **200W** CONVERTER

R1, 2	825k	1%
R3, 4	243k	1%
R5	42.2k	1%
R6, 7	10k	
R8	10.0k	1%
R9	15.0k	1%
R10, 11	62k	1w
R12	68	
R13	36k	
R14	39k	
R15,23	2k	
R16, 17	15k	3w
R18	10	2w
R19, 20	33	1/2w
R21	33	
R22	200	
R24	18.7k	1%
R25	6.49k	1%
R26	1k	
R27, 28	20	
R29	100	
R30, 31	120k	1/2w
R32	5ΩNTC	thermistor

C1-C4	390µF	20%	200V
C5	100µF	20%	25V
C6, 20, 31, 32, 35, 38	1µF		
C7, 14	1nF		
C8	220pF	5%	
C9	47nF		
C10	390pF	5%	
C11	22pF		
C12	330pF		
C13	220pF		
C15	10nF		
C16	2.2nF		
C17	4.7nF		100V
C18, 19	470pF		500V
C21, 23	3.3nF		
C24-C30	1000µF	20%	10V
C32, 33, 36, 37	330µF	20%	25V
C39, 40	2.2nF	20%	500V
	class x/y		
C41, 42	100nF	20%	100V

D1	MB106-ND	(Diodes, Inc.)
D2, 3	1N5820	
D3	1N4745A	
D4, 5	1N4148	
D6	10DF8	(International Recifier)
D7	40CPQ060	(International Recifier)
D9, 10	10CTF20	(International Recifier)
Q1	APT801R2BN	(Advanced Power Technology)
L1, 2	RL-1160-1.0	(Renco)
L3	SHFI-2515	(Signal Transformer Co.)
TR1	SHF-2525-16	(Signal Transformer Co.)
TR2	PE64978	(Pulse Engineering)
U1	UC3848	
U2	UC19432	

NOTE: All resistors 5%, 1/4 watt unless noted
All capacitors 10%, 50V unless noted

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